

# OKI semiconductor

## MSM5278

### DOT MATRIX LCD 64 DOT COMMON DRIVER

#### GENERAL DESCRIPTION

The OKI MSM5278GS is a dot matrix LCD's common driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 64-bit bidirectional shift register, 64-bit level shifter and 64-bit 4-level driver.

This LSI has 64 output pins to be connected to the LCD. By connecting more than two MSM5278GSs in series, this LSI is applicable to a wide LCD panel.

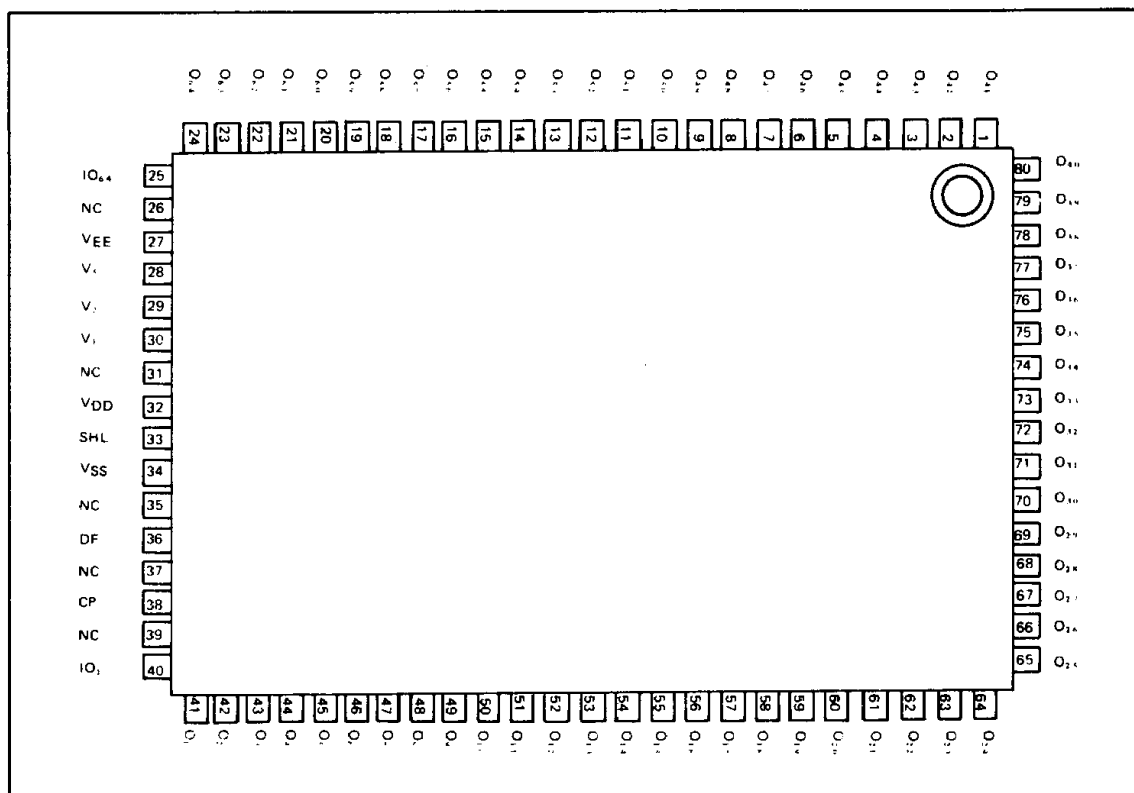
This LSI can drive a variety of LCD because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

#### FEATURES

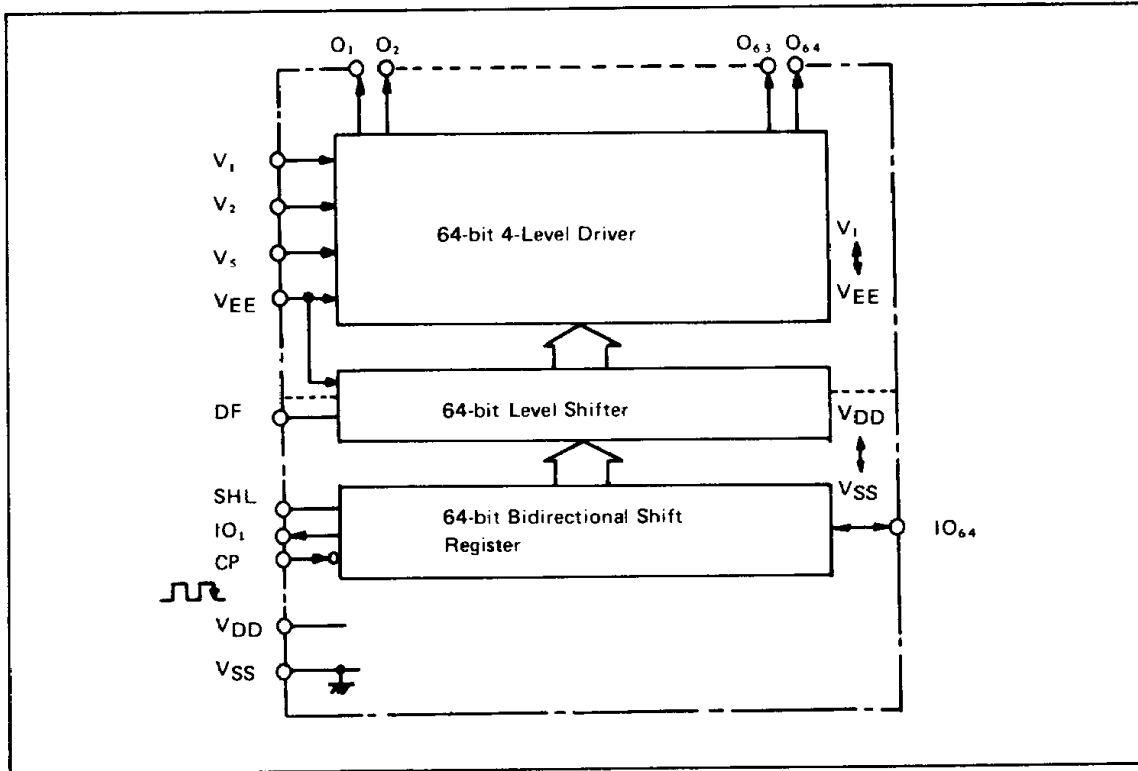
- Supply voltage: 4.5 ~ 5.5V
  - LCD driving voltage: 8 ~ 20V
  - Applicable LCD duty: 1/64 ~ 1/128
  - Bias voltage can be supplied externally
  - 80 pin plastic QFP (QFP80-P-1420-K)
- Two chips of the MSM5278GS are required to drive 1/128 duty LCD.

#### PIN CONFIGURATION

(Top view) 80 pin plastic QFP



**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V <sub>DD</sub>	T <sub>a</sub> = 25°C	-0.3 ~ 6	V
Supply voltage (2)	V <sub>DD</sub> - V <sub>EE</sub> *1	T <sub>a</sub> = 25°C	0 ~ 22	V
Input voltage	V <sub>I</sub>	T <sub>a</sub> = 25°C	-0.3 ~ V <sub>DD</sub> + 0.3	V
Storage temperature	T <sub>stg</sub>	—	-55 ~ + 150	°C

\*1 V<sub>1</sub> > V<sub>2</sub> > V<sub>3</sub> > V<sub>EE</sub>, V<sub>1</sub> ≤ V<sub>DD</sub>

**OPERATING RANGE**

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V <sub>DD</sub>	—	4.5 ~ 5.5	V
Supply voltage (2)	V <sub>DD</sub> - V <sub>EE</sub> *1	—	8 ~ 20	V
Operating temperature	T <sub>op</sub>	—	-20 ~ + 85	°C

\*1 V<sub>1</sub> > V<sub>2</sub> > V<sub>3</sub> > V<sub>EE</sub>, V<sub>1</sub> ≤ V<sub>DD</sub>

### D.C. CHARACTERISTICS

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -20 \sim +85^\circ C$ )

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	$V_{IH}^{*1}$	—	$0.8V_{DD}$	—	—	V
"L" Input voltage	$V_{IL}^{*1}$	—	—	—	$0.2V_{DD}$	V
"H" Input current	$I_{IH}^{*1}$	$V_{IH} = V_{DD}$	—	—	1	$\mu A$
"L" Input current	$I_{IL}^{*1}$	$V_{IL} = 0V$	—	—	-1	$\mu A$
"H" Output voltage	$V_{OH}^{*2}$	$I_O = -0.4mA$	$V_{DD}-0.4$	—	—	V
"L" Output voltage	$V_{OL}^{*2}$	$I_O = 0.4mA$	—	—	0.4	V
ON Resistance	$R_{ON}^{*4}$	$V_{DD} - V_{EE} = 18V$ *3 $ V_N - V_O  = 0.25V$	—	1	2	$k\Omega$
Power consumption	$I_{DD}$	CP = DC $V_{DD} - V_{EE} = 18V$ No load	—	—	100	$\mu A$
Input capacitance	$C_I$	$f = 1MHz$	—	5	—	pF

\*1 Application to CP, IO<sub>1</sub>, IO<sub>64</sub> SHL and DF terminals.

\*2 Applicable to IO<sub>1</sub>, and IO<sub>64</sub> terminals.

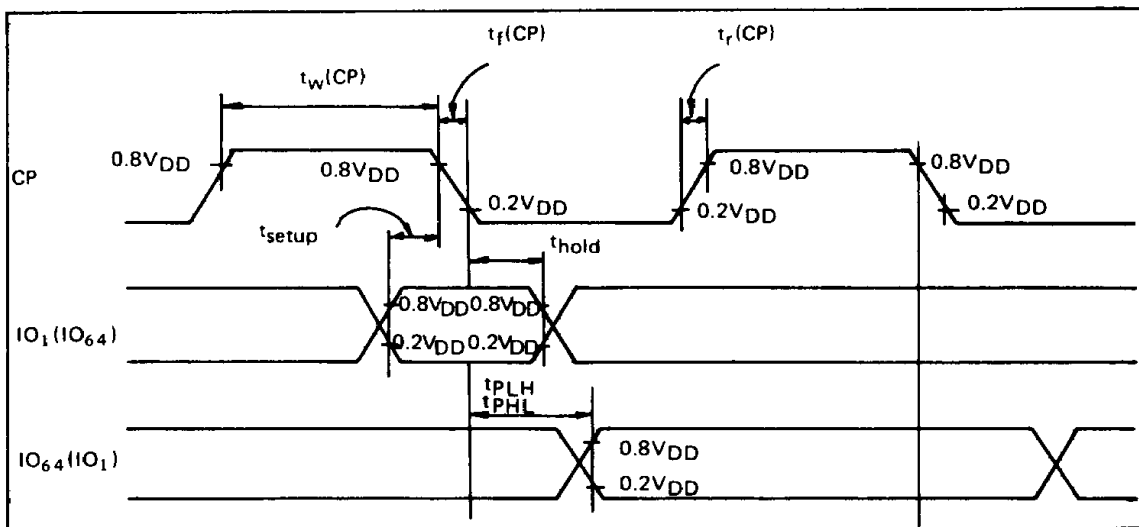
\*3  $V_N = V_{DD} \sim V_{EE}$ ,  $V_2 = \frac{10}{11} (V_{DD} - V_{EE})$ ,  $V_5 = \frac{1}{11} (V_{DD} - V_{EE})$ ,  $V_{DD} = V_1$

\*4 Applicable to O<sub>1</sub> ~ O<sub>64</sub> terminals.

### SWITCHING CHARACTERISTICS

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -20 \sim +85^\circ C$  CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" "L" propagation delay time	$t_{PLH}$ $t_{PHL}$	—	—	—	250	ns
Max. clock frequency	$f_{CP}$	—	1	—	—	MHz
Clock pulse width	$t_w(CP)$	—	125	—	—	ns
Data set-up time IO <sub>1</sub> (IO <sub>64</sub> ) → CP	$t_{setup}$	—	100	—	—	ns
Data hold time IO <sub>1</sub> (IO <sub>64</sub> ) → CP	$t_{hold}$	—	100	—	—	ns
Clock pulse Rising/Falling time	$t_r(CP)$ $t_f(CP)$	—	—	—	50	ns



**PIN DESCRIPTION**

● **IO<sub>1</sub>, IO<sub>64</sub>, SHL**

IO<sub>1</sub> and IO<sub>64</sub> are 64-bit bidirectional shift register input/output pins. The shifting direction is selected

by the H/L condition of SHL pin. Refer to the table below.

SEL	Shifting direction	IO <sub>1</sub> /IO <sub>64</sub>	Input/output	Pin description
L	O <sub>1</sub> → O <sub>64</sub>	IO <sub>1</sub>	Input	The scanning data from the LCD controller LSI is input from IO <sub>1</sub> synchronized with the clock pulse. *1
		IO <sub>64</sub>	Output	Shift register contents output pin. The data which was input from IO <sub>1</sub> is output from IO <sub>64</sub> with 64 bits' delay, synchronized with the clock pulse. Refer to the application circuit.
H	O <sub>64</sub> → O <sub>1</sub>	IO <sub>64</sub>	Input	The scanning data from the LCD controller LSI is input from IO <sub>64</sub> synchronized with the clock pulse. *1
		IO <sub>1</sub>	Output	Shift register contents output pin. The data which was input from IO <sub>64</sub> is output from IO <sub>1</sub> with 64 bits' delay, synchronized with the clock pulse. Refer to the application circuit.

\*1 The combination of the scanning data, IO<sub>1</sub> or IO<sub>64</sub>, and the LCD driving output, O<sub>1</sub> ~ O<sub>64</sub>, is shown in the table below.

IO <sub>1</sub> , IO <sub>64</sub>	LCD driving output
H	Selected level (V <sub>1</sub> , V <sub>EE</sub> )
L	Non-selected level (V <sub>2</sub> , V <sub>5</sub> )

● **CP**

Clock pulse input pin for 64-bit bidirectional shift register. The data is shifted to 64-bit level shifter at the falling edge of the clock pulse.

● **DF**

Alternate signal input pin for LCD driving. Normal frame inversion signal is input.

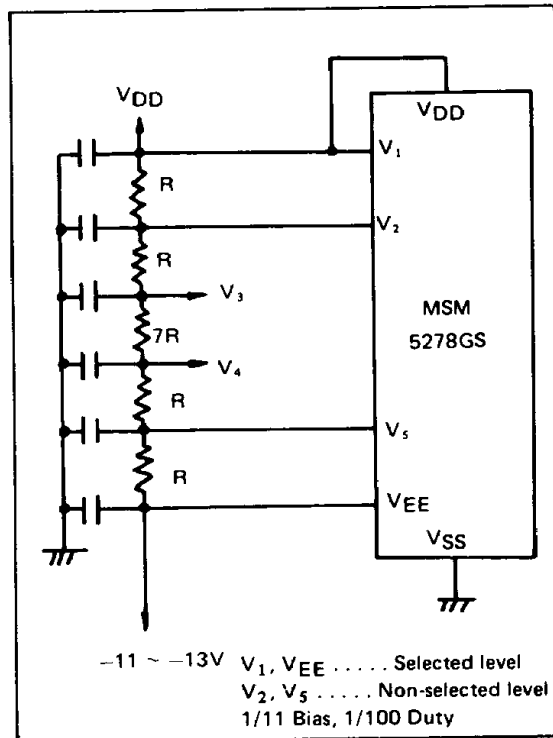
● **V<sub>DD</sub>, V<sub>SS</sub>**

Supply voltage pins. V<sub>DD</sub> should be 4.5 ~ 5.5V. V<sub>SS</sub> is a ground pin. (V<sub>SS</sub> = 0V)

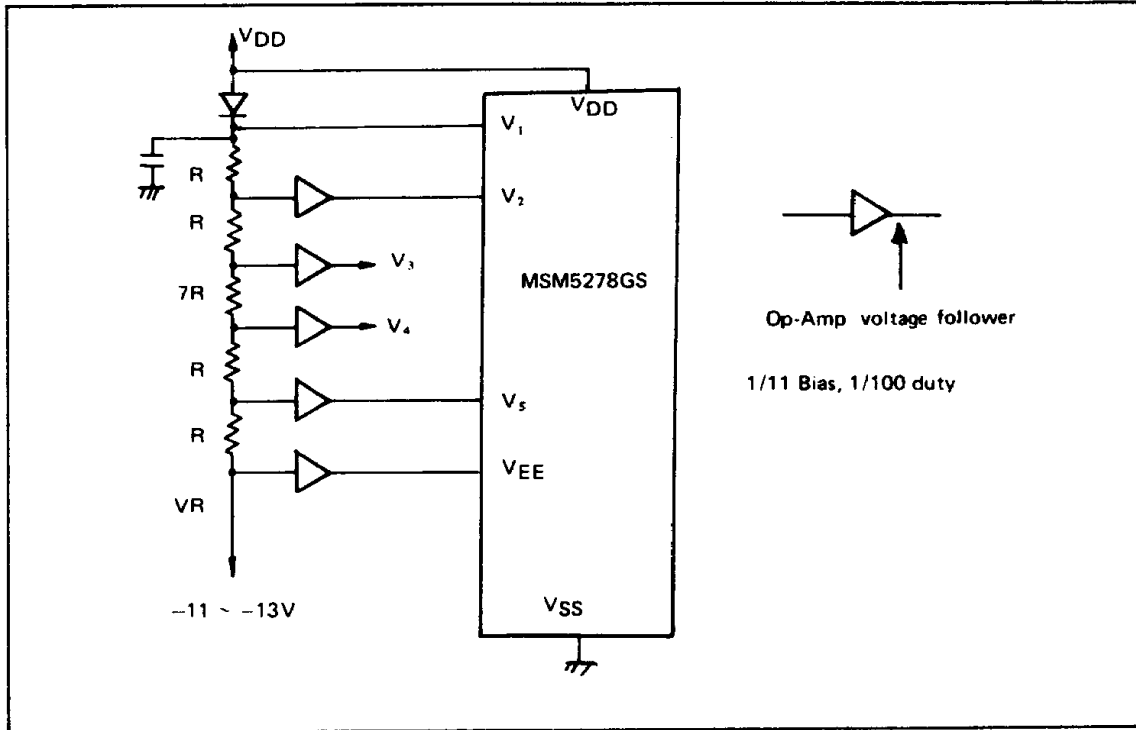
● **V<sub>1</sub>, V<sub>2</sub>, V<sub>5</sub>, V<sub>EE</sub>**

Bias supply voltage pins to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.

The below figure shows the case when bias voltage is divided by the resistance. V<sub>1</sub> is not necessarily connected to V<sub>DD</sub>.



The figure below shows the case when bias voltage is supplied by the Op-Amps. By using Op-Amps, the bias voltage becomes low impedance and the power consumption of MSM5278 becomes low.



●  $O_1 \sim O_{64}$

Display data output pins which correspond to 64-bit shift register contents. One of  $V_1$ ,  $V_2$ ,  $V_5$  and  $V_{EE}$  is selected as a display driving voltage

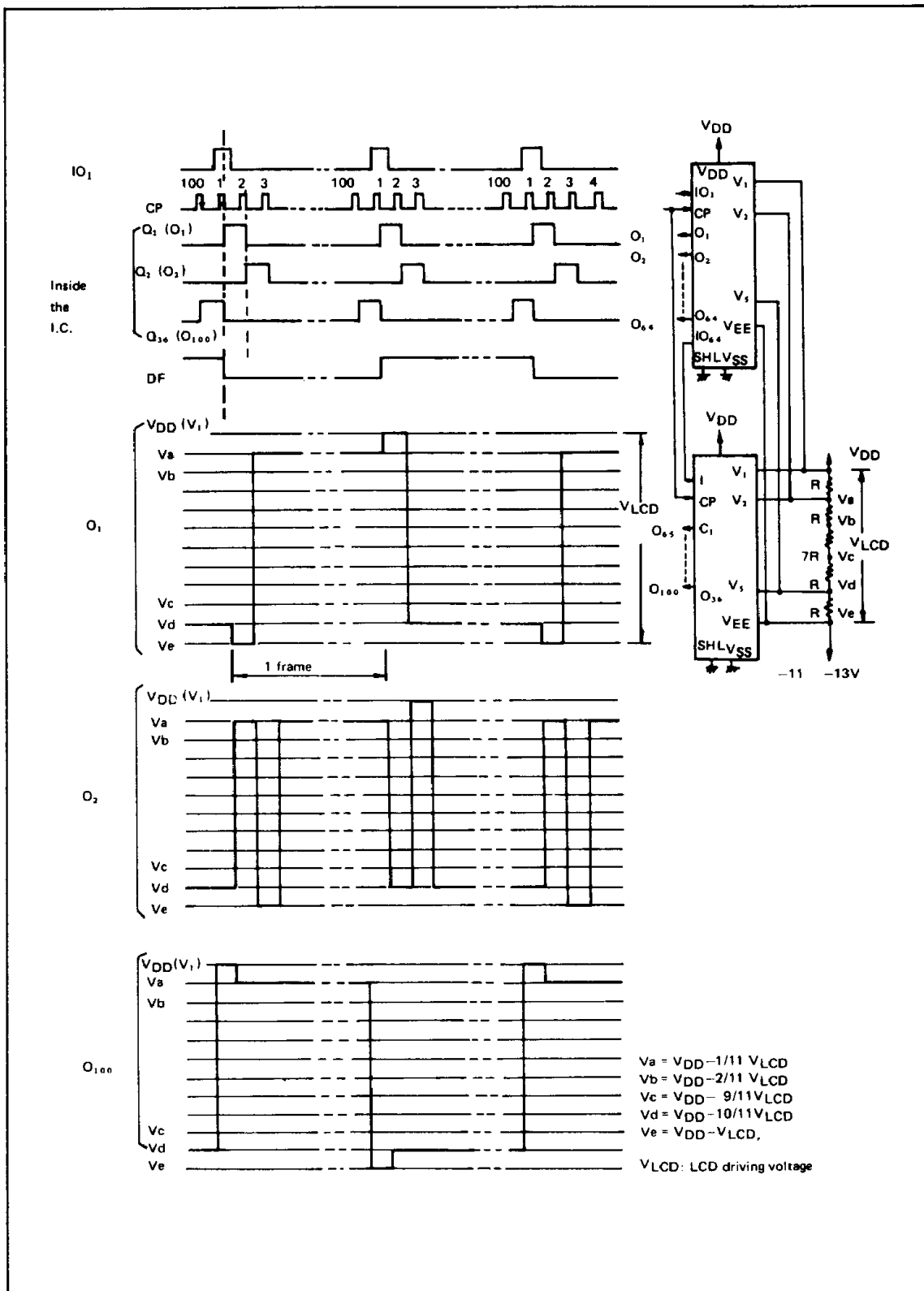
source according to the combination of the latched data level and DF signal. (Refer to the truth table below.)

DF	Latched data level	Display data output level ( $O_1 \sim O_{64}$ )
L	L	$V_2$
L	H	$V_{EE}$
H	L	$V_5$
H	H	$V_1$

Truth table

### TIMING CHART

1/100 duty, 1/11 bias



APPLICATION CIRCUIT

